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ENGINEERING SPECIFICATIONS

Product Name:

CA3-8DXXX

M.2 PCIe Gen3 x 4 Lane SSD

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Version	History	Date
1.0	First Release	2017/04/21
1.1	區分 CA3-8DXXX 跟 CA3-GDXXX 機種	2017/12/22
1.2	Update SED specification	2018/01/22
1.3	Update Performance IOMeter Information	2018/03/30

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1 INTRODUCTION

1.1 Overview:

The CA3-8DXXX PCIe Gen3 x 4 Lane series Solid State Drive (SSD) delivers leading performance in an industry standard M.2 type 2280-S3-M form factor while simultaneously improving system responsiveness for applications over standard rotating drive media or hard disk drives. By combining leading NAND flash memory technology with our innovative high performance firmware, LITEON delivers a SSD for PCIe hard disk drive drop-in replacement with enhanced performance, reliability, ruggedness and power savings. Since there are no rotating platters, moving heads, fragile actuators, or unnecessary delays due to spin-up time or positional seek time that can slow down the storage subsystem, significant I/O and throughput performance improvement is achieved as compared to rotating media or hard disk drives. This document describes the specifications of the CA3-8DXXX PCIe Gen3 x 4 Lane series M.2 SSD in M.2 type 2280-S3-M form factors.

The CA3-8DXXX PCIe Gen3 x 4 Lane series M.2 SSD primarily targets M.2 based laptop PCs, highly rugged client devices, as well as thin and light mini/sub-notebooks. Key attributes include high performance, low power, increased system responsiveness, high reliability, and enhanced ruggedness as compared to standard hard drives. The CA3-8DXXX PCIe Gen3 x 4 Lane series M.2 SSD is available in M.2 type 2280-S3-M form factor that are electrically, mechanically, and software compatible with existing M.2 slots. Our flexible design allows interchangeability with existing hard drives based on the M.2 interface standard.

The CA3-8DXXX series SED SSD is a TCG/Opal v2.01 compliant self-encrypting drive (SED). It adopts hardware-based AES-256 encryption for all data stored in drive with no performance degradation. The encryption keys are generated in the drive and never leave the drive. The drive provides a secure boot capability (re-boot authentication) as well as protection of user data from compromise due to the loss, theft, repurposing, or end of life of the storage device. It also provides administrative capabilities that allow administrative functions such as user enrollment and media management.

1.2 Product Specification

1.2.1. Form Factor: M.2 type 2280-S3-M SSD form factor

1.2.2. Capacity: available now

M.2 2280-S3-M 256/512GB (CA3-8D256/512)

Table 1 User Addressable Sectors

Unformatted capacity	Total user addressable sectors in LBA mode
256GB	500,118,192
512GB	1,000,215,216

Notes:

- 1). 1GB=1,000,000,000 bytes and not all of the memory can be used for storage.
- 2). 1 Sector = 512 bytes

1.2.3. Flash:

Triple-Level Cell (TLC) component with Toggle-Mode

1.2.4. Band Performance

Table 2 Maximum Sustained Read and Write Bandwidth on Windows 10 platform

Capacity	Access Type	MB/s
256 GB	Sequential Read	2800
	Sequential Write	800
	Sequential Write (TLC mode)	280
512 GB	Sequential Read	3000
	Sequential Write	1600
	Sequential Write (TLC mode)	500

Notes:

- 1). Performance measured using Crystal Disk Mark 5.0.2, QD32 T1, 1GiB test size, 5 cycles.
- 2). PCIe link speed is gen3x4.
- 3). Write cache enabled & 4K boundary data.
- 4). Test by secondary drive (data drive & clean state).
- 5). Performance based on internal testing on X1-Carbon 5th Windows 10; Performance may vary on different platforms, NVMe driver and OS.

1.2.5. Read and Write IOPS

Table 3 Random Read/Write Input/Output Operations per Second on Windows 10 platform

Capacity	Access Type	IOPS
256 GB	4K Read (IOPS)	150K
	4K Write (IOPS)	140K
512 GB	4K Read (IOPS)	250K
	4K Write (IOPS)	220K

Notes:

- 1). Performance measured using Crystal Disk Mark 5.0.2, QD32 T4, 1GiB test size, 5 cycles.
- 2). Test by secondary drive (data drive & clean state).
- 3). PCIe link speed is gen3x4.
- 4). Performance based on internal testing on X1-Carbon 5th Windows 10; Performance may vary on different platforms, NVMe driver and OS.

Table 4.1 Random Read/Write Input/Output Operations per Second on Windows 10 platform

Capacity	Access Type	IOPS
256 GB	4K Read (IOPS)	100K
	4K Write (IOPS)	60K
512 GB	4K Read (IOPS)	130K
	4K Write (IOPS)	80K

Notes:

- 1). Performance measured using Lenovo IOMeter script, QD64 T1 (Logical Disk with full span).
- 2). Performance based on internal testing on X1-Carbon 5th Windows 10; Performance may vary on different platforms, NVMe driver and OS.

1.2.6. Ready Time

Table 5 Latency Specifications

Type	Average Latency
Power on to Ready	1 sec

Notes:

- 1). Write cache enabled
- 2). Device measured using Drive Master
- 3). PCIe link speed is gen3x4.
- 4). Test results may be different on different platform.
- 5). Power on to ready time assumes proper shutdown
(Power removal preceded by host Shutdown Notification)

1.2.7. Compatibility

- NVM Express Specification
- PCI Express Base Specification
- PCI Express M.2 Electromechanical Specification
- Microsoft latest WHCK Certification
- Support Legacy and UEFI BIOS
- TCG/Opal SSC v2.01 rev 1.00 compliance for SED drive
- TCG Storage Interface Interactions Specification (SIIS) ver 1.05 rev 1.00 compliance for SED drive

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1.2.8. Supported Operating System and Chipset

--Operating System

Windows 7 x86, x64 / Windows 8 x86, x64 / Windows 10

Linux series, Red Hat 6.5, Fedora, SUSE, Ubuntu

Windows Server 2008, 2012

--Chipset:

※Please make sure the BIOS of the used mother board be updated to the latest version.

1.2.9. Certifications

Table 5 Device Certifications

Certification	Description
CE compliant	Indicates conformity with the essential health and safety requirements set out in European Directives Low voltage Directive and EMC Directive
UL certified	Underwriters Laboratories, Inc. Component Recognition UL60950-1
BSMI	Compliance to the Taiwan EMC standard "Limits and methods of Radio Disturbance Characteristics of Information Technology Equipment, CNS 13438 Class B"
Microsoft WHQL	Microsoft Windows Hardware Quality Labs
RoHS compliant	Restriction of Hazardous Substance Directive

1.2.10. PCIe M.2 interface Power Management

3.3V Input/ Max current (RMS): 3A

1.2.11. Power Consumption

Table 6 Operating Voltage & Current

Description	Min	Max	Unit
Operating voltage for 3.3V (+/- 5%)	3.135	3.465	V

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Table 7 Power Consumption

Capacity	Operation	Max	Unit
512 GB	Start-up	6	W
	Read-Write	8	W

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1.2.12. Temperature

Table 8 Temperature Relative Specifications

Environment	Mode	Min	Max	Unit
Ambient Temperature	Operating	0	70	°C
	Non-operating	-40	85	°C
Humidity	Operation	5	95	%
	Non-operation	5	95	%

Note:

Measured without condensation

1.2.13. Reliability

Table 9 Reliability specifications

Parameter	Value
Mean Time between Failure (MTBF) ¹	>2,000,000 hours
Power on/off cycle ²	50,000 cycles

Notes:

- 1). MTBF is calculated based on a Part Stress Analysis. It assumes nominal voltage with all other parameters within specified range.
- 2). Power on/off cycles is defined as power being removed from the drive, and the restored. Most host systems remove power from the drive when entering suspend and hibernate as well as on a system shutdown.

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1.2.14. Shock and Vibration

Table 10 Shock and Vibration

Item	Mode	Timing/Frequency	Max
Shock ¹	Non-operating	At 0.5 msec half-sine	1500G
Vibration ²	Non-operation	2-500 Hz	3.1 Grms

Notes:

1). Shock specifications assume that the SSD is mounted securely with the input vibration applied to the drive mounting screws. Stimulus may be applied in the X, Y or Z axis.

2). Vibration specifications assume that the SSD is mounted securely with the input vibration applied to the drive mounting screws. Stimulus may be applied in the X, Y or Z axis. The measured specification is in root mean squared form.

1.2.15. Electrostatic discharge (ESD)

Electromagnetic Immunity tests assume the SSD is properly installed in the representative host system. The drive operates properly without errors degradation in performance when subjected to radio frequency (RF) environments defined in the following table.

Table 11 Radio Frequency Specifications

Test	Description	Performance criteria	Reference standard
Electrostatic discharge	Contact $\pm 4\text{KV}$ Air: $\pm 8\text{KV}$	A	IEC 61000-4-2:2008
Electrostatic discharge	Contact $\pm 6\text{KV}$ Air: $\pm 12\text{KV}$	B	IEC 61000-4-2:2008
Electrostatic discharge	Contact $\pm 8\text{KV}$ Air: $\pm 15\text{KV}$	C	IEC 61000-4-2:2008
Radiated RF immunity	80~1000MHz, 3V/m, 80% AM with 1 KHz sine 900 MHz, 3 V/m, 50% pulse modulation at 200Hz	A	IEC 61000-4-3:2008
Electrical fast transient	$\pm 1\text{KV}$ on AC mains $\pm 0.5\text{KV}$ on external I/O	B	IEC 61000-4-4:2004 +Corr.1:2006 +Corr.2:2007
Surge immunity	$\pm 1\text{KV}$ differential $\pm 2\text{KV}$ common, AC mains	B	IEC 61000-4-5:2005
Conducted RF immunity	150KHz~80 MHz, 3 Vrms, 80% AM with 1KHz sine	A	IEC 61000-4-6:2008
Power frequency magnetic field	50Hz, 1A/m (r.m.s.)	A	IEC 61000-4-6:2008

Notes:

1. Performance criterion A = The device shall continue to operate as intended, i.e., normal unit operation with no degradation of performance.
2. Performance criterion B = The device shall continue to operate as intended after completion of test, however, during the test, some degradation of performance is allowed as long as there is no data loss operator intervention to restore device function.
3. Performance criterion C = Temporary loss of function is allowed. Operator intervention is acceptable to restore device function.
4. Contact electrostatic discharge is applied to drive enclosure.

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1.2.16. Weight:

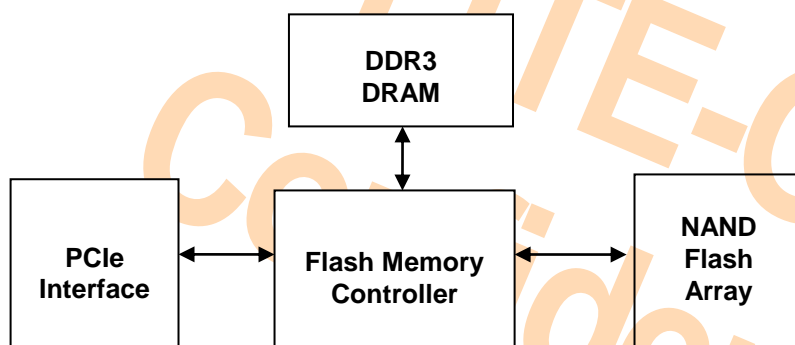
Weight spec. = 10 g Max. (CA3-8DXXX)

1.2.17. Dimension:

Form factor:

M.2 2280: 80.0 mm x 22.0 mm x 2.30 mm (L x W x H) (CA3-8DXXX)

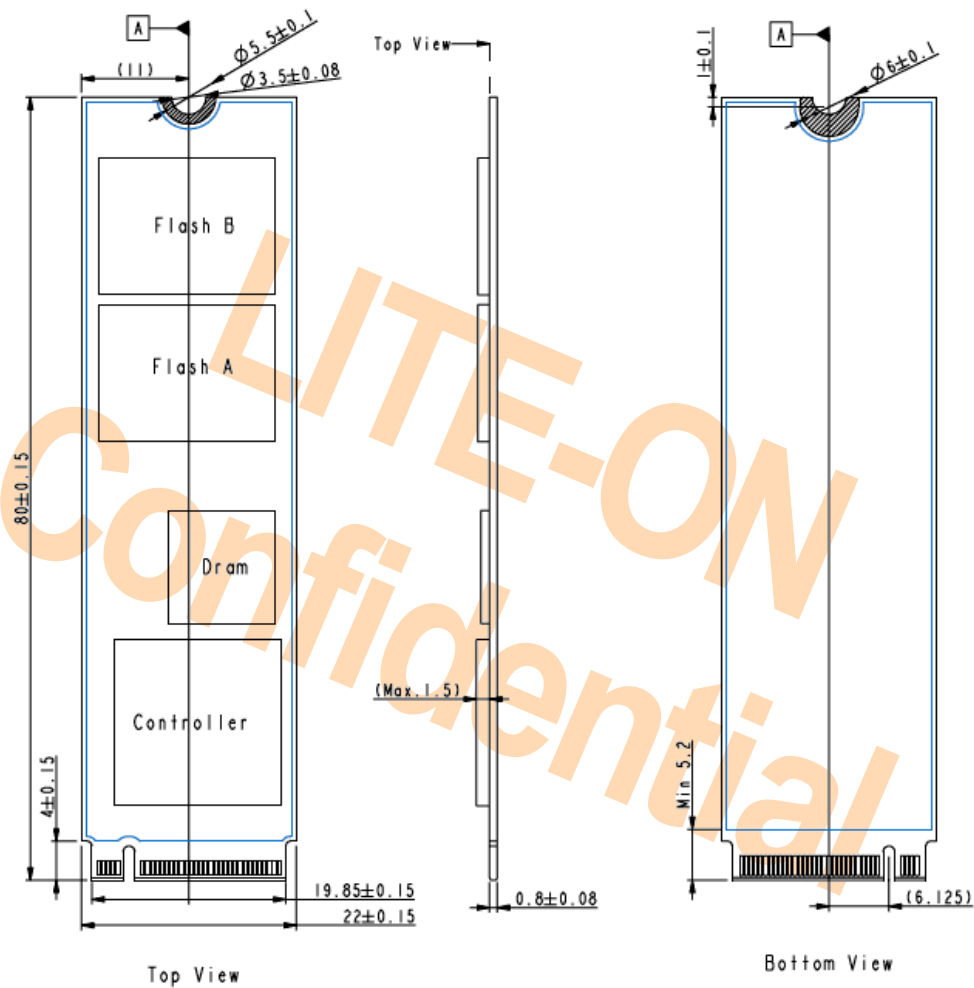
1.3 Functional Block Diagram



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1.4 Mechanical Drawing:

M.2 2280-S3-M: CA3-8DXXX



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1.5 Architecture

The CA3-8DXXX PCIe Gen3 x 4 Lane Solid State Drive (SSD) utilizes a cost effective system-on-chip (SoC) design to provide a full 4GB/s bandwidth with the host while managing multiple flash memory devices on multiple channels internally.

1.6 Bootable Device:

The CA3-8DXXX PCIe Gen3 x 4 Lane Solid State Drive (SSD) is configured as a bootable device. This supported function allows users to manage it as a main system drive and to boot from PCIe SSD.

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1.7 Power Mode Support

PCI Express feature enables the hardware to engage actively in automatic Link power management.

CA3-8DXXX PCIe Gen3 x 4 Lane SSD Supports L0, L0s and L1 mode.

-L0: Full On (Active power / Active mode)

-L0s: Idle (Lower power / Idle mode)

-L1: Idle (Lower power / sleep mode)

The Link state transits automatically from L0 (full on) to an L0s/L1 (idle) state to save power when there is no data transferring. The device reduces power by gating internal clocks, and the CLKREQ# signal transited by host will enable lower power mode of some internal components such as PCIe PHY. Once the data can be transferred across the Link, the state will be brought back to L0 by the hardware.

Table 12 Radio Frequency Specifications

Input Voltage	State			1024 GB (W)
3.3V ± 5%	Active Mode (L0 state)	After power-on		2.4
		Max. Read/Write Performance	rms	8
	Idle Mode (L0s state)			2.8
	Sleep Mode (L1.2 state)			0.01

※L0 stands for power states after power-on and before entering L0s/L1,

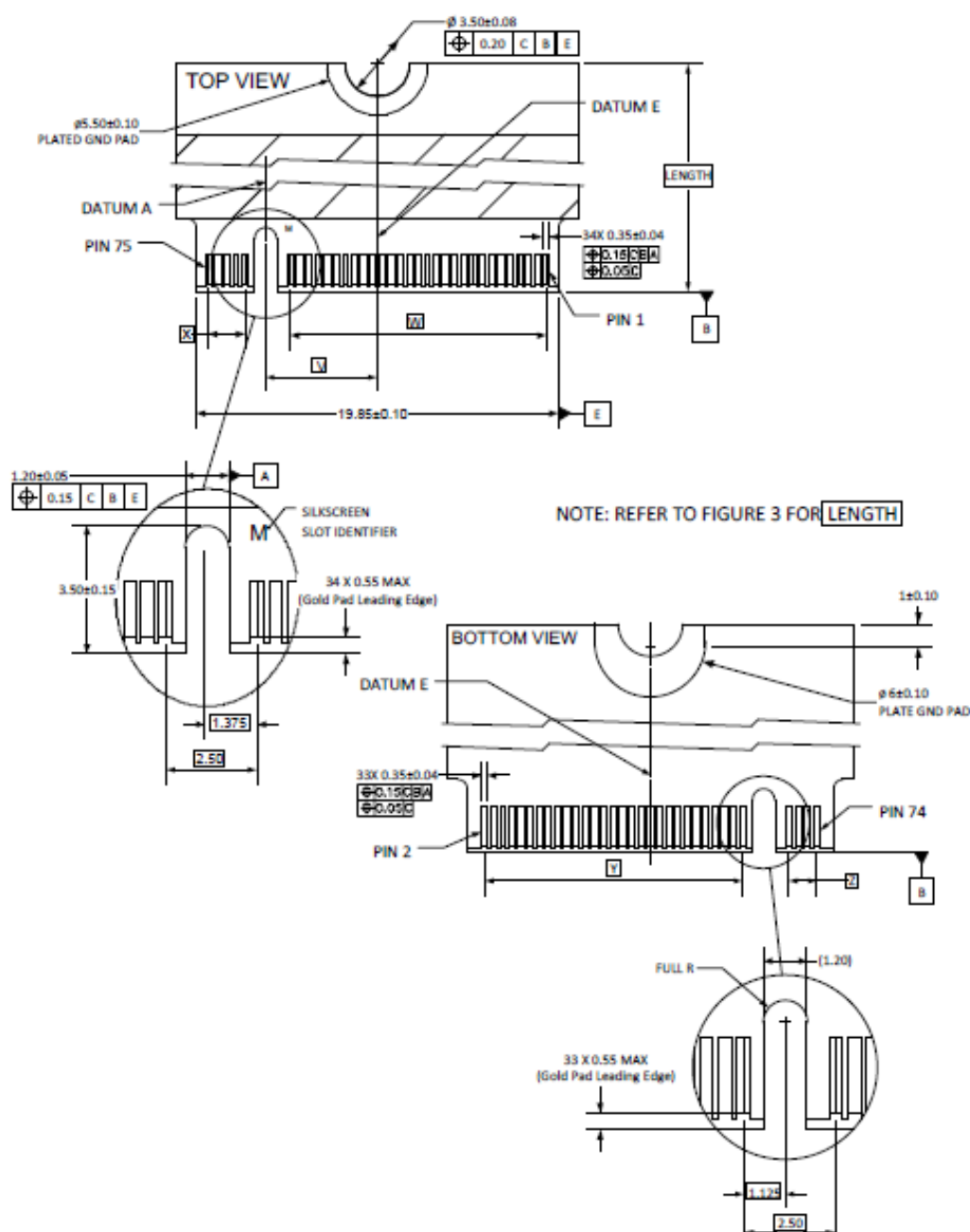
※To enable L1 lower mode, the CLKREQ# signal must be sent by host.

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2 PIN LOCATIONS AND SIGNAL DESCRIPTIONS

2.1 Pin Locations

The data and power connector pin locations of the CA3-8DXXX PCIe SSD Gen3 x 4 Lane are shown below. This M.2 device contains Socket 3 + M key.



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2.2 M.2 Socket Definition

The PCI Express interface supported in Socket 3 is a 4 Lane PCI Express interface intended for premium SSD devices that need this sort of host interface.

	Soldered-down			Connectorized			
	Type	Module Height Options	Pinout Key	Connector Key	Type	Module Height Options	Module Key
Socket 1 Connectivity	1216	S1, S3	E	N/A	N/A	N/A	N/A
	N/A	N/A	N/A	A, E	1630	S1, D1, S3, D3, D4	A, E, A+E
	2226	S1, S3	E	A, E	2230	S1, D1, S3, D3, D4	A, E, A+E
	3026	S1, S3	A+E	A, E	3030	S1, D1, S3, D3, D4	A, E, A+E
Socket 2 WWAN/Other	N/A	N/A	N/A	B	3042	S1, D1, S3, D3, D4	B
Socket 2 SSD/Other	N/A	N/A	N/A	B	2230	S2, D2, S3, D3, D5	B+M
	N/A	N/A	N/A	B	2242	S2, D2, S3, D3, D5	B+M
	N/A	N/A	N/A	B	2260	S2, D2, S3, D3, D5	B+M
	N/A	N/A	N/A	B	2280	S2, D2, S3, D3, D5	B+M
	N/A	N/A	N/A	B	22110	S2, D2, S3, D3, D5	B+M
Socket 3 SSD Drive	N/A	N/A	N/A	M	2242	S2, D2, S3, D3, D5	M, B+M
	N/A	N/A	N/A	M	2260	S2, D2, S3, D3, D5	M, B+M
	N/A	N/A	N/A	M	2280	S2, D2, S3, D3, D5	M, B+M
	N/A	N/A	N/A	M	22110	S2, D2, S3, D3, D5	M, B+M

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2.3 Socket 3 PCIe-based SSD Module Pinout

74	3.3V	GND	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK	PEDET	69
		N/C	67
	Key	Key	
	Key	Key	
	Key	Key	
	Key	Key	
58	Reserved	GND	57
56	Reserved	REFCLKp	55
54	PEWAKE#	REFCLKn	53
52	CLKREQ#	GND	51
50	PERST#	PERp0	49
48	N/C	PERn0	47
46	N/C	GND	45
44	ALERT#	PETp0	43
42	SMB_DATA	PETn0	41
40	SMB_CLK	GND	39
38	N/C	PERp1	37
36	N/C	PERn1	35
34	N/C	GND	33
32	N/C	PETp1	31
30	PLP_FBCK	PETn1	29
28	N/C	GND	27
26	N/C	PERp2	25
24	N/C	PERn2	23
22	N/C	GND	21
20	N/C	PETp2	19
18	3.3V	PETn2	17
16	3.3V	GND	15
14	3.3V	PERp3	13
12	3.3V	PERn3	11
10	LED#	GND	9
8	PLP_INIT	PETp3	7
6	N/C	PETn3	5
4	3.3V	GND	3
2	3.3V	GND	1

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3 PCI EXPRESS

3.1 Interface

The PCI Express interface supports the x1 PCI Express interface (one Lane). A Lane consists of an input and an output high-speed differential pair. Also supported is a PCI Express reference clock. Refer to the PCI Express Base Specification for more details on the functional requirements for the PCI Express interface signals.

Socket 1 pin out has provisions for an additional PCI Express lane indicated by the suffix 1 to the signal names. These additional PETx1 and PERx1 signal sets can serve as the second Lane to the original PCI Express interface, or alternatively, they can be complimented with a second set of REFCLKx1 and a set of Auxiliary Signals on the adjacent reserved pins to form a complete second PCI Express x1 interface.

3.2 Auxiliary Signals

The auxiliary signals are provided on the system connector to assist with certain system level functionality or implementation. These signals are not required by the PCI Express architecture, but may be required by specific implementations such as PCI Express M.2 Card. The high-speed signal voltage levels are compatible with advanced silicon processes. The optional low speed signals are defined to use the +3.3V supply, as it is the lowest common voltage available. Most ASIC processes have high voltage (thick gate oxide) I/O transistors compatible with +3.3V. The use of the +3.3V supply allows PCI Express signaling to be used with existing control bus structures, avoiding a buffered set of signals and bridges between the buses.

The PCI Express M.2 Card add-in card and system connectors support the auxiliary signals that are described in the following sections.

3.3 Reference Clock

The REFCLK+/REFCLK- signals are used to assist the synchronization of the card's PCI Express interface timing circuits. Availability of the reference clock at the card interface may be gated by the CLKREQ# signal as described in section 3.1.5.1, CLKREQ# Signal. When the reference clock is not available, it will be in the parked state. A parked state is when the clock is not being driven by a clock driver and both REFCLK+ and REFCLK- are pulled to ground by the ground termination resistors. Refer to the PCI Express Card Electromechanical Specification for more details on the functional and tolerance requirements for the reference clock signals.

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3.3.1 CLKREQ# Signal

The CLKREQ# signal is an open drain, active low signal that is driven low by the PCI Express M.2 add-I Card function to request that the PCI Express reference clock be available (active clock state) in order to allow the PCI Express interface to send/receive data. Operation of the CLKREQ# signal is determined by the state of the Enable Clock Power Management bit in the Link Control Register (offset 010h). When disabled, the CLKREQ# signal shall be asserted at all times whenever power is applied to the card, with the exception that it may be de-asserted during L1 PM Sub states. When enabled, the CLKREQ# signal may be de-asserted during the L1 Link state.

The CLKREQ# signal is also used by the L1 PM Sub states mechanism. In this case, CLKREQ# can be asserted by either the system or add-in card to initiate an L1 exit. See the PCI Express Base Specification for details on the functional requirements for the CLKREQ# signal when implementing L1 PM Sub states.

Whenever dynamic clock management is enabled and when a card stops driving CLKREQ# low, it indicates that the device is ready for the reference clock to transition from the active clock state to a parked (not available) clock state. Reference clocks are not guaranteed to be parked by the host system when CLKREQ# gets de-asserted and module designs shall be tolerant of an active reference clock even when CLKREQ# is de-asserted by the module.

The card must drive the CLKREQ# signal low during power up, whenever it is reset, and whenever it requires the reference clock to be in the active clock state. Whenever PERST# is asserted, including when the device is not in D0, CLKREQ# shall be asserted.

It is important to note that the PCI Express device must delay de-assertion of its CLKREQ# signal until it is ready for its reference clock to be parked. The device must be able to assert its clock request signal, whether or not the reference clock is active or parked, when it needs to put its Link back into the L0 Link state. Finally, the device must be able to sense an electrical idle break on its up-stream-directed receive port and assert its clock request, whether or not the reference clock is active or parked.

The assertion and de-assertion of CLKREQ# are asynchronous with respect to the reference clock. Add-in cards that do not implement a PCI Express interface shall leave this output unconnected on the card. CLKREQ# has additional electrical requirements over and above standard open drain signals that allow it to be shared between devices that are powered off and other devices that may be powered on. The additional requirements include careful circuit design to ensure that a voltage applied to the CLKREQ# signal network never causes damage to a component even if that particular component's power is not applied.

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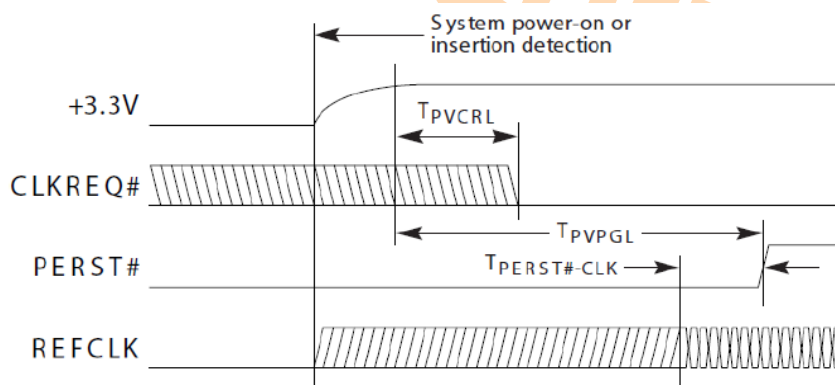
Additionally, the device must ensure that it does not pull CLKREQ# low unless CLKREQ# is being intentionally asserted in all cases; including when the related function is in D3cold. This means that any component implementing CLKREQ# must be designed such that:

- Unpowered CLKREQ# output circuits are not damaged if a voltage is applied to them from other powered “wire-Red” sources of CLKREQ#.
- When power is removed from its CLKREQ# generation logic, the unpowered output does not present a low impedance path to ground or any other voltage.

These additional requirements ensure that the CLKREQ# signal network continues to function properly when a mixture of powered and unpowered components have their CLKREQ# outputs wire-ORed together. It is important to note that most commonly available open drain and tri-state buffer circuit designs used “as is” do not satisfy the additional circuit design requirements for CLKREQ#.

3.3.2 Power-up Requirements

CLKREQ# is asserted in response to PERST# assertion. On power up, CLKREQ# must be asserted by a PCI Express device within a delay (TPVCRL) from the power rails achieving specified operating limits and PERST# assertion (see Figure 78). This delay is to allow adequate time for the power to stabilize on the card and certain system functions to start prior to the card starting up. CLKREQ# may not be de-asserted while PERST# is asserted.



Note: TPVCRL is measured from the later rising edge of +3.3V.

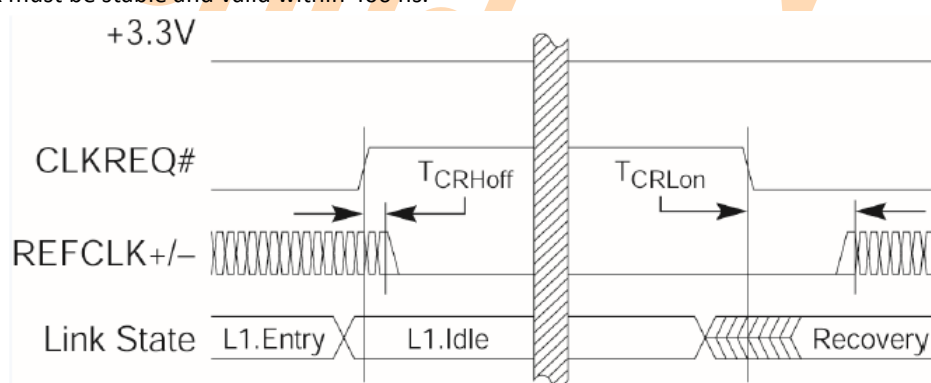
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3.3.3 Dynamic Clock Control

After a PCI Express device has powered up and whenever its upstream link enters the L1 link state, it shall allow its reference clock to be turned off (put into the parked clock state). To accomplish this, the device de-asserts CLKREQ# (high) and must allow that the reference clock will transition to the parked clock state within a delay (T_{CRHoff}). Figure 79 shows the CLKREQ# clock control timing diagram.

To exit L1, the device must assert CLKREQ# (low) to re-enable the reference clock. After the device asserts CLKREQ# (low) it must allow that the reference clock will continue to be in the parked clock state for a delay (T_{CRLon}) before transitioning to the active clock state. The time that it takes for the device to assert CLKREQ# and for the system to return the reference clock to the active clock state are serialized with respect to the remainder of L1 recovery. This time must be taken into account when the device is reporting its L1 exit latency.

When the PCI Express device supports, and is enabled for, Latency Tolerance Reporting (LTR), the device must allow that the reference clock transition to the active clock state may be additionally delayed by the system up to a maximum value consistent with requirements for the LTR mechanism. During this delay, the reference clock must remain parked. When exiting the parked state following the delay, the clock must be stable and valid within 400 ns.



3.3.4 Clock Request Support Reporting and Enabling

Support for the CLKREQ# dynamic clock protocol should be reported using bit 18 in the PCI Express link capabilities register (offset 0C4h). To enable dynamic clock management, bit 8 of the Link Control register (offset 010h) is provided. By default, the card shall enable CLKREQ# dynamic clock protocol upon initial power up and in response to any warm reset by the host system. System software may subsequently disable this feature as needed. Refer to the PCI Express Base Specification, Revision 1.1 (or later) for more information regarding these bits.

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3.3.5 PERST# Signal

- The PERST# signal is de-asserted to indicate when the system power sources are within their specified voltage tolerance and are stable.
- PERST# should be used to initialize the card functions once power sources stabilize.
- PERST# is asserted when power is switched off and also can be used by the system to force a hardware reset on the card.
- System may use PERST# to cause a warm reset of the add-in card.

Refer to the PCI Express Card Electromechanical Specification for more details on the functional requirements for the PERST# signal.

3.3.6 WAKE# Signal

PCI Express M.2 Cards must implement WAKE# if the card supports either the wakeup function or the OBFF mechanism. Refer to the PCI Express Card Electromechanical Specification for more details on the functional requirements for the WAKE# signal.

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4 ADMIN COMMAND SETS

4.1 Admin Command

The CA3-8DXXX PCIe Gen3 x4 Lane SSD supports all the mandatory Admin commands defined in the NVMe 1.2 specification which consists of

- Delete I/O Submission Queue
- Create I/O Submission Queue
- Get Log Page
- Delete I/O Completion Queue
- Create I/O Completion Queue
- Identify
- Abort
- Set Features
- Get Features
- Asynchronous Event Request

The CA3-8DXXX PCIe Gen3 x 4 Lane SSD supports all the following optional commands

- Namespace Management
- Firmware Commit
- Firmware Image Download
- Namespace Attachment
- Security Send
- Security Receive

4.2 Namespace Feature Set

The Namespace Management command is used to create a namespace or delete a namespace. The Namespace Attachment command is used to attach and detach controllers from a namespace. Namespace management is intended for use during manufacturing or by a system administrator.

When a namespace is detached from a controller or deleted it becomes an inactive namespace on that controller. Previously submitted but uncompleted or subsequently submitted commands to the affected namespace are handled by the controller as if they were issued to an inactive namespace.

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4.3 Security Feature Set

The Security Receive command transfers the status and data result of one or more Security Send commands that were previously submitted to the controller.

The association between a Security Receive command and previous Security Send commands is dependent on the Security Protocol. The format of the data to be transferred is dependent on the Security Protocol. Refer to SPC-4 for Security Protocol details.

Each Security Receive command returns the appropriate data corresponding to a Security Send command as defined by the rules of the Security Protocol. The Security Receive command data may not be retained if there is a loss of communication between the controller and host, or if a controller reset occurs.

The Security Send command is used to transfer security protocol data to the controller. The data structure transferred to the controller as part of this command contains security protocol specific commands to be performed by the controller. The data structure transferred may also contain data or parameters associated with the security protocol commands. Status and data that is to be returned to the host for the security protocol commands submitted by a Security Send command are retrieved with the Security Receive command.

5 NVMe COMMAND SETS

5.1 NVMe Command

The CA3-8DXXX PCIe Gen3 x4 Lane SSD supports all the mandatory NVMe commands defined in the NVMe 1.2 specification, which consists of

- Flush
- Write
- Read

The CA3-8DXXX PCIe Gen3 x 4 Lane SSD supports all the following optional commands

- Write Uncorrectable
- Dataset Management

5.2 Power Management Feature Set

The power management capability allows the host to manage NVM subsystem power statically or dynamically. Static power management consists of the host determining the maximum power that may be allocated to an NVM subsystem and setting the NVM Express power state to one that consumes this amount of power or less. Dynamic power management consists of the host modifying the NVM Express power state to best satisfy changing power and performance objectives. This power management mechanism is meant to complement and not replace autonomous power management performed by a controller.

Associated with each power state is a Power State Descriptor in the Identify Controller data structure. The descriptors for all implemented power states may be viewed as forming a table as shown for a controller with three implemented power states. The Maximum Power (MP) field indicates the instantaneous maximum power that may be consumed in that state. The controller may employ autonomous power management techniques to reduce power consumption below this level, but under no circumstances is power allowed to exceed this level.

Power State	Maximum Power	Operational State	Entry Latency	Exit Latency
0	8W	Yes	<5us	<5us
3	50mW	No	<1ms	<10ms
4	10mW	No	<5ms	<40ms

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6 REFERENCES

This document references standards defined by a variety of organizations as listed below.

Table 63 Standards References

Title	Location
VCCI	http://www.vcci.or.jp/vcci_e/general/join/index.html
ROHS	Search for material description datasheet at http://intel.pcnaalert.com
PCI Express Specification	http://www.pcisig.com
PCI Express M.2 Specification	https://pcisig.com/specifications/pciexpress/M.2_Specification/
NVM Express Specification	http://www.nvmexpress.org
International Electro Technical Commission EB61000 4-2 Personnel Electrostatic Discharge Immunity 4-3 Electromagnetic compatibility (EMC) 4-4 Electromagnetic compatibility (EMC) 4-5 Electromagnetic compatibility (EMC) 4-6 Electromagnetic compatibility (EMC) 4-11 (Voltage variations)	http://www.iec.ch
ENV 50204 (Radiated electromagnetic field from digital radio telephones)	http://www.iec.ch
TCG Storage Security Subsystem Class: Opal Version 2.01, Revision 1.00	http://www.trustedcomputinggroup.org
TCG Storage Interface Interactions Specification (SIIS) Version 1.05, Revision 1.00	http://www.trustedcomputinggroup.org

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7 TERMS AND ACRONYMS

This document incorporates many industry- and device-specific words use the following list to define a variety of terms and acronyms.

Table 74 Glossary of Terms and Acronyms

Term	Definition
BER	Bit Error Rate, or percentage of bits that have errors relative to the total number of bits received
BIOS	Basic Input/Output System
Chipset	A term used to define a collection of integrated components required to make a PC function
DRAM	Dynamic Random Access Memory
GB	Giga-byte defined as 1×10^9 bytes
IOPS	Input output operations per second
LBA	Logical Block Address
MB	Mega-bytes defined as 1×10^6 bytes
MTBF	Mean time between failure
OS	Operation System
SSD	Solid State Drive
WHQL	Microsoft* Windows Hardware Quality Labs
Write Cache	A memory device within a hard drive, which is allocated for the temporary storage of data before that data is copied to its permanent storage location
VCCI	Voluntary Control Council for Interface
A	Amperage or Amp
GND	Ground
I/F	Interface
I/O	Input/Output
LED	Light Emitting Diode
mΩ	milli Ohm
mA	milli Amp
mV	milli Volt
M.2	Formally called Next Generation Form Factor (NGFF)
NC	Not Connected
PCIe	Peripheral Component Interconnect Express
SSD	Sold-State Storage Device
RF	Radio Frequency
RM	Root Mean Square
RoHS	Restriction of Hazardous Substances Directive
V	Voltage
W	Wattage or Watts